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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,401	10/22/2003	Philip Ngai	97703	6808

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EXAMINER	
FLOURNOY, HORACE L	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/691,401	NGAI ET AL.	
	Examiner	Art Unit	
	Horace L. Flournoy	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 are presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1- 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Ichiriu et al. (U.S. Patent No. 6,597,595 hereafter referred to as Ichiriu).

With respect to independent claim 1,

> "An apparatus for identifying matching items, the apparatus comprising: an associative memory bank, including an ordered plurality of entries, for generating matching indication signals for each matching entry of the ordered plurality of entries that matches a lookup value;" is disclosed in the abstract and column 20, lines 56-58.

Ichiriu discloses in the abstract, "A content addressable memory (CAM) device having a data CAM array and an error CAM array. The data CAM array is provided to store data words, compare the data words with a comparand value, and, if one of the data words matches the comparand value, assert a match signal that corresponds to the matching data word. A priority encoder responds to the match signal by outputting a match address that corresponds to the matching data word." Ichiriu also discloses in column 20, lines 56-58, "Any order of significance may be assigned to the row, segment and block addresses in alternative embodiments."

Ichiriu teaches an apparatus for identifying matching items (CAM), the apparatus comprising: an associative memory bank (CAM), including an ordered plurality of entries (any order of significance may be assigned to the row, segment and block addresses in alternative embodiments), for generating matching indication signals for each matching entry of the ordered plurality of entries that matches a lookup value (assert a match signal that corresponds to the matching data word).

> "...and a merging mechanism, coupled to the matching mechanism, for identifying a winning entry from said matching entries, wherein each of the ordered plurality of entries is associated with (a) one of an ordered plurality of groups and (b) a skip or a no-skip condition" is disclosed in column 5, lines 22-26, column 8, lines 29-36, 2-8 and FIGs. 1-6.

Ichiriu discloses in column 5, lines 22-26, "The highest priority match (HPM) register 121 is loaded (e.g., under control of the instruction decoder) with a CAM index

174 generated during a compare operation and therefore points to the CAM word that produced the highest priority match in the most recent compare operation." Ichiriu next discloses in column 8, lines 29-36, "As shown, a CAM word formed by of N groups of M data bits is output from the sense amplifier bank 162. The first group of data bits is designated D[M-1, 0], the second group of data bits is designated D[(2.times.M)-1, M] and so forth to the final group of data bits designated D[(N.times.M)-1, (N-1).times.M]. The CAM word also includes N parity bits, one for each group of M bits." Ichiriu also discloses in column 8, lines 2-8, "The skip bit indicates that the corresponding row of CAM cells are to be skipped (i.e., ignored) during a compare operation, while the empty bit indicates that no CAM word is stored in the corresponding row of CAM cells. Thus, the skip bit and the empty bit are each reset to indicate that a valid CAM word is stored in the corresponding row of CAM cells."

Ichiriu teaches a merging mechanism, coupled to the matching mechanism (FIGs.1-6), for identifying a winning entry from said matching entries (highest priority match register), wherein each of the ordered plurality of entries is associated with one of an ordered plurality of groups (a CAM word formed by of N groups of M data bits) and a skip or a no-skip condition (the skip bit indicates that the corresponding row of CAM cells are to be skipped).

"...and wherein the merging mechanism selects the winning entry based on said matching indication signals;" is disclosed as stated supra in the abstract.

"...wherein said selecting the winning entry includes identifying as the winning entry an entry of said matching entries first in the priority ordering of the ordered plurality of entries that is not in a group that is skipped," is disclosed in column 7, lines 60-67 and column 8, lines 1-12.

The examiner interprets this limitation as first identifying the winning entry or best match from priority group that is not skipped.

Ichiriu discloses in column 7, lines 61-67, "In a first state (i.e., when set), the validity bit indicates that the corresponding row of CAM cells contains a valid CAM word. Conversely, in a second state (i.e., when reset), the validity bit indicates that the corresponding row of CAM cells does not contain a valid CAM word. In alternative embodiments, two or more bits may be used to represent the validity value. For example, in one alternative embodiment, the validity value is formed by a pair of bits: a skip bit and an empty bit." Ichiriu also discloses in column 8, lines 2-8, "The skip bit indicates that the corresponding row of CAM cells are to be skipped (i.e., ignored) during a compare operation, while the empty bit indicates that no CAM word is stored in the corresponding row of CAM cells. Thus, the skip bit and the empty bit are each reset to indicate that a valid CAM word is stored in the corresponding row of CAM cells."

Ichiriu teaches first identifying (a first state (i.e., when set), the validity bit indicates that the corresponding row of CAM cells contains a valid CAM word) the winning entry or best match from priority group that is not skipped (skip bit is reset).

"...wherein a particular group is skipped if the highest priority matching entry of the particular group is associated with a skip condition." is disclosed as stated supra.

With respect to independent claims 5, 9, 11, 13, 15, 17, 19

"An apparatus for identifying matching items, the apparatus comprising: an associative memory bank, including an ordered plurality of entries, for generating matching indication signals for each matching entry of the ordered plurality of entries that matches a lookup value;" is disclosed in the abstract and column 20, lines 56-58 (see claim 1).

"...and a merging mechanism, coupled to the matching mechanism, for identifying a winning entry from said matching entries, wherein each of the ordered plurality of entries is associated with (a) one of an ordered plurality of hierarchical first groups, (b) one of an ordered plurality of hierarchical second groups, (c) a skip or a no-skip first-level condition, and (d) a skip or a no-skip second-level condition, and..." is disclosed as stated supra in claim 1 and in column 18, lines 39-42.

Ichiriu discloses in column 18, lines 39-42, "The position of the matching column within the parity check matrix (i.e., first column, second column, etc.) corresponds to the position of the bit in error within the CAM word 503."

Note: the examiner notes that Ichiriu discusses a first column, second column etc. which correspond to hierarchical first and second groups. It is also noted that these columns or groups can utilize the skip bit.

"...wherein the merging mechanism selects the winning entry based on said matching indication signals; wherein said selecting the winning entry includes identifying as the winning entry an entry of said matching entries first in the priority ordering of the ordered plurality of entries that is not in a group of the hierarchical first or second groups that is skipped" is disclosed as stated supra and in claim 1 and in column 18, lines 39-42.

"...wherein a particular first group of the first hierarchical groups is skipped if the highest priority matching entry of the particular first group is associated with a skip first-level condition, and a particular second group of the second hierarchical groups is skipped if the highest priority matching entry of the particular second group is associated with a skip second-level condition." Is disclosed in column 7, lines 61-67 and column 8, lines 2-8.

Ichiriu discloses in column 7, lines 61-67, "In a first state (i.e., when set), the validity bit indicates that the corresponding row of CAM cells contains a valid CAM word. Conversely, in a second state (i.e., when reset), the validity bit indicates that the corresponding row of CAM cells does not contain a valid CAM word. In alternative embodiments, two or more bits may be used to represent the validity value. For

example, in one alternative embodiment, the validity value is formed by a pair of bits: a skip bit and an empty bit." Ichiriu also discloses in column 8, lines 2-8, "The skip bit indicates that the corresponding row of CAM cells are to be skipped (i.e., ignored) during a compare operation, while the empty bit indicates that no CAM word is stored in the corresponding row of CAM cells. Thus, the skip bit and the empty bit are each reset to indicate that a valid CAM word is stored in the corresponding row of CAM cells."

Ichiriu teaches a particular first group of the first hierarchical groups (first column) is skipped if the highest priority matching entry of the particular first group is associated with a skip first-level condition (first state), and a particular second group (second column) of the second hierarchical groups is skipped if the highest priority matching entry of the particular second group is associated with a skip second-level condition (second state).

With respect to claims 3 and 7,

"The apparatus of claim 1(5), wherein each of the plurality of groups corresponds to a different access control list." is disclosed in column 8, lines 40-46.

Ichiriu discloses in column 8, lines 40-46.The data and parity bits are input to a parity check circuit 201 that includes a separate parity generator 206 and compare circuit 208 for each group of data bits and its corresponding parity bit. Each parity generator 206 generates a binary output according to the state of an even/odd select

signal 232 and the number of set (or reset) data bits within the corresponding group of data bits.

Ichiriu teaches packet classification utilizing separate parity generator and compare circuits for each group.

With respect to claims 4 and 8,

"The apparatus of claim 1(5), wherein the merging mechanism includes circuitry for identifying and masking skipped entries of said matching entries is disclosed in column 3, lines 61-64 and column 23, lines 7-13.

Ichiriu discloses in column 3, lines 61-64, "During a compare operation, the comparand may be masked by a global mask value, then compared simultaneously with all the CAM words stored in the CAM array 101." Ichiriu further discloses in column 23 lines 7-13, "If, during a given compare operation, a highest priority match is detected between a comparand value and a corrupted CAM word, the resulting match index may be invalid (i.e., if the defective bits within the corrupted CAM word are not masked in the compare operation, the match index will have resulted from a false match and therefore will be invalid).

Ichiriu teaches circuitry for identifying and masking skipped entries of said matching entries (column 23 lines 7-13). Ichiriu teaches that entries can be skipped via the skip bit as stated supra.

With respect to claims 6 and 2,

"The apparatus of claim 5, comprising one or more banks of one or more storage elements for identifying for each particular entry of the plurality of entries: (a) the associated skip or no-skip first-level condition, (b) the associated skip or no-skip second-level condition," is disclosed as stated supra in claim 5.

Note: The examiner notes that a CAM comprises one or more banks of one or more storage elements for identifying for each particular entry of the plurality of entries.

"...(c) whether or not said particular entry is first in the order sequence of one of the ordered plurality of hierarchical first groups, and (c) whether or not said particular entry is first in the order sequence of one of the ordered plurality of hierarchical second groups." is disclosed as stated supra in claims 1 and 5.

Ichiriu discloses in column 10, lines 35-37, "The multiple-entry error address register 289 preferably operates as a first-in-first-out (FIFO) storage having head and tail entries."

With a FIFO storage Ichiriu teaches how to determine whether or not said particular entry is first in the order sequence of one of the ordered plurality of hierarchical first or second groups.

With respect to claims 10, 12, 14, 16, 18, and 20

"The method of claim 9, wherein said identifying as the winning entry includes masking one or more of said received indications of said matching entries of in a group that is skipped. " is disclosed in column 3, lines 61-64 and column 23, lines 7-13.

The examiner interprets claims 10, 12, 14, 16, 18, and 20 as winning or best match identification includes masking one or more of the received indications of the matching entries of a group that is skipped.

Ichiriu discloses in column 3, lines 61-64, "During a compare operation, the comparand may be masked by a global mask value, then compared simultaneously with all the CAM words stored in the CAM array 101." Ichiriu further discloses in column 23 lines 7-13, "If, during a given compare operation, a highest priority match is detected between a comparand value and a corrupted CAM word, the resulting match index may be invalid (i.e., if the defective bits within the corrupted CAM word are not masked in the compare operation, the match index will have resulted from a false match and therefore will be invalid).

Ichiriu teaches the winning or best match identification (compare operation) includes masking one or more of the received indications of the matching entries (During a compare operation, the comparand may be masked by a global mask value) of a group that is skipped. Note: as noted above Ichiriu also discloses in column 8, lines 2-8, "The skip bit indicates that the corresponding row of CAM cells are to be skipped (i.e., ignored) during a compare operation, while the empty bit indicates that no CAM word is stored in the corresponding row of CAM cells. Thus, the skip bit and the empty

bit are each reset to indicate that a valid CAM word is stored in the corresponding row of CAM cells." Ichiriu teaches a group can be skipped.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere* CO., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 13 and 19 are rejected under 35 U.S.C. 103(a) as being obvious over Ichiriu (U.S. Patent no. 6,597,595) in view of "Structured Computer Organization" 2nd edition, by Tanenbaum (hereafter referred to as Tanenbaum).

With further respect to independent claims 13 and 19, Ichiriu does not disclose expressly, "A computer readable medium containing computer-executable instructions for performing steps for identifying matching items..."

Tanenbaum discloses, "*Hardware and software are logically equivalent.* Any operation performed by software can also be built directly into the hardware and any instruction executed by the hardware can also be simulated in software" (page 11).

Ichiriu and Tanenbaum are analogous art because they are from the same field of endeavor, that being computer architecture.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate the apparatus for identifying matching items (hardware) as a computer program product to arrive at claims 13 and 19.

The motivation for doing so would have been obvious based on the teaching of Tanenbaum on page 11 "*Hardware and software are logically equivalent.* Any operation performed by software can also be built directly into the hardware and any instruction executed by the hardware can also se simulated in software."

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement claims 1, 5, 9, 11, 15, and 17 in software thereby obtaining the inventions as specified in claims 13 and 19.

Conclusion

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday-Friday 7:00 AM to 4:30 PM (ET).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Sparks can be reached on (571) 272-4201. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Horace L. Flournoy
Patent Examiner
Art unit: 2189

CHRISTIAN CHACE
PRIMARY EXAMINER

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